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Application Note

How to Use STARC with Cryptographic Tags in a One-wire Configuration

Introduction

Using cryptographic transponders assumes the ability to transmit data to the transponder and to read its answer. A one-wire configuration is a Stand-Alone Tag-Reader Circuit (STARC) operation mode which is cost-effective because it requires one or two wires less than other market solutions and uses a less expensive connector.

However, a designer should be aware of potentially severe application issues. These issues may result from transmitting (or receiving) transponder data and STARC control data on the same wire. If the STARC is not used properly, the transponder communication may collapse in a one wire configuration.

This Application Note proposes solutions to potential application issues when using the STARC in a one-wire configuration. Using these solutions eliminates disturbed transponder communication.

STARC Timing Values

The following STARC timing values are defined:

- t_{ref} is the STARC oscillator period; ideally 125 ns.
- $t_{driver} = 64 * t_{ref}$
- T0 = 8192 * t_{ref}; ideally 1.024 ms. This is the maximum time for the STARC to switch in write (read) when K = 0 (=1).
- T1 = 8.064* t_{ref}; ideally 1.008 ms. This is the minimum time for the STARC to switch in write (read) when K = 0 (=1).
- T = 8128 * t_{ref}; typically T = 1.016 ms.

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When the STARC antenna signal is not modulated, the output of the demodulator is random. This random output can be any of the following:

- High; the demodulator comparator offset is positive.
- Low; the demodulator comparator offset is negative.
- Noisy; the demodulator comparator offset is very close to 0 mV.

Random output occurs when no transponder is present in the H field and or when the transponder does not answer.

As a consequence, when there is no antenna modulation and when K is not pulled down by the remote Body Controller Module (BCM) Microcontroller Unit (MCU), one of the following STARC configurations results:

- Write mode and K = 1. The timing value is not longer than T0 because the STARC switches into read mode as soon as K = 1 for more than T0.
- Read mode and K = 1 (it is the demodulator output); there is no upper limit.
- Read mode and K = 0 (it is the demodulator output). The timing value is not longer than T0 because the STARC switches into write mode as soon as K = 0 for more than T0.

Thus, when there is no transponder answer and when the K line is let free by the BCM MCU, the STARC has one of the following responses:

- Remains in read mode (the demodulator comparator offset is always positive); K is high.
- Toggles from write to read and read to write with a mean period of T per mode. (For example, 1.016 ms typically; the demodulator comparator offset is negative.) The K line looks like a square wave signal with a frequency that is typically 1/2T = 500 Hz.
- Remains in read mode; however, the K line is noisy. The minimum noise pulse is t_{driver} because the demodulator comparator output is latched with a clock period whose period is t_{driver}.

The STARC can also alternate with these cases. Thus, the STARC state of the machine is not controlled and is unknown if the K line is not monitored.

Read to Write Switching

To force the STARC into write mode from read mode requires that K = 0 for T0. This condition can be met when K is pulled down by the demodulator, the remote BCM MCU, or both. What matters is that the total time K = 0 (whatever the device which pulls down K).

Therefore, pulling down K without monitoring the K line is risky, because the STARC can toggle in write earlier than expected, as shown in Figure 1.

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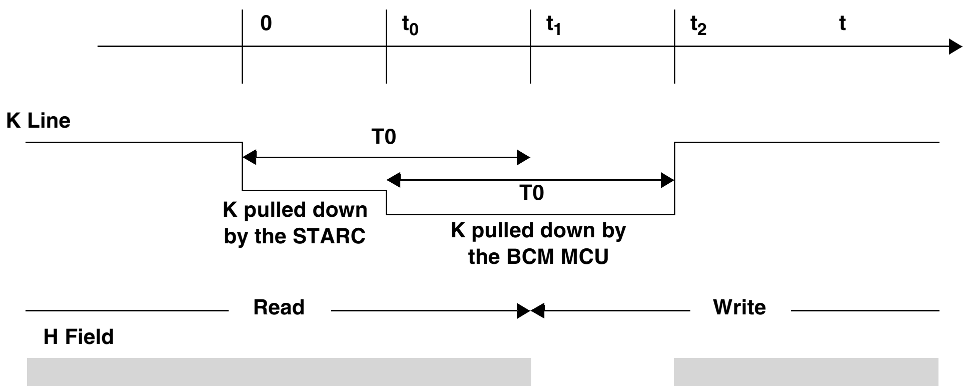

Figure 1.

As shown in Figure 1, the STARC is initially in read mode; the demodulator output is low so that K = 0. Then the BCM MCU pulls down for T0, from the time $t = t_0$. The cumulative T0 time with K = 0 is reached when $t = t_1$. The STARC then toggles in write mode at $t = t_1$, instead of the expected $t= t_2$.

As a consequence, the H field is then switched off because K controls the STARC antenna drivers in write mode and K = 0. The shut down of the H field is unexpected and unwanted and puts the transponder into trouble. (The shut down of the H field may either reset the transponder if it is too long, or be interpreted as a first challenge data).

Therefore, it is recommended to monitor the K line before sending the write command pulse. It is suggested that the following test be implemented before the BCM MCU pulls down the K line.

1. Wait until K = 1.
2. Start a ΔT time-out loop ($\Delta T > T0$) with two exit following conditions.
   — The ΔT time-out occurs
   — A falling edge on K is detected

As a result of this test, the ΔT time-out occurs, or a falling edge on K is detected.

The first condition always occurs (at least after T0 ms) if the K line is let free. The STARC state of the machine is still unknown at this step. If the loop is exited when the time-out occurs, then K was high for more than T0. This is possible only if the STARC was in read mode when the loop was started and if the STARC has remained in read mode for the entire time-out.

If the loop is exited because a falling edge is detected, it means that K was pulled down by the demodulator and then the STARC toggled into read mode.

Therefore, when this test sequence is complete, the STARC is in read mode. K is either high or has just been pulled down. Then the BCM MCU can pull down the K line for toggling the STARC in write mode. But it is mandatory that this occurs without any delay so that the total cumulative time, where K = 0, is controlled by the BCM MCU.

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Read to Write Switching

The write command pulse duration must also be controlled. As a matter of fact, if it is longer than T0, the H field is switched off after T0. The transponder is either reset or interprets the H field shut-down as first challenge data (Figure 2).

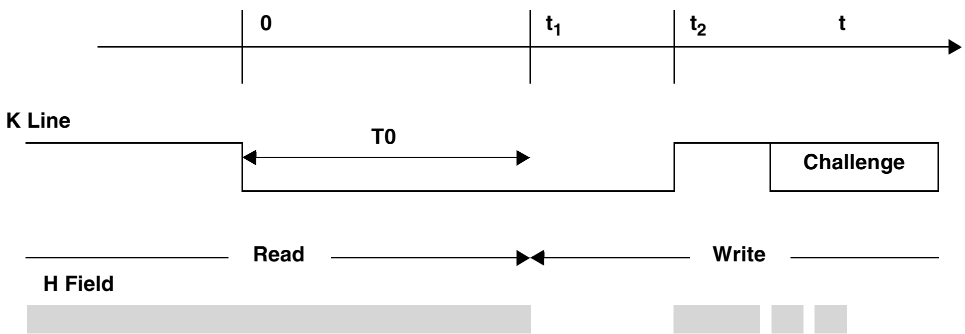

Figure 2.

As shown in Figure 2, the write command pulse is longer than T0. The STARC toggles into write mode at $t = t_1$. As $K = 0$, the H field is shut-down until $t = t_2$, although no data is being transmitted.

Therefore, it is recommended to concatenate the low pulse of the first challenge data with the write command pulse.

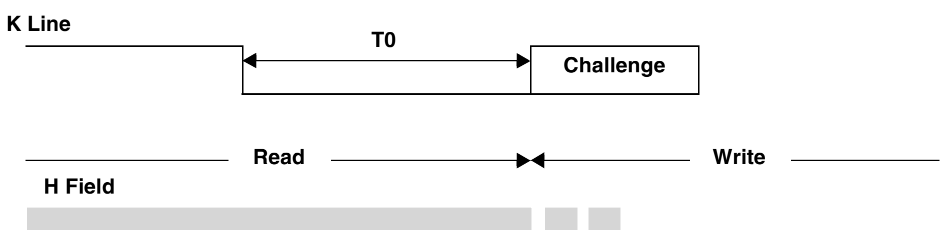

Figure 3.

The length of the write command will then be:

- $T_{write} = T' + t_0$,
  - T' being as close as possible to T
  - t_0 being the typical pulse length of the negative pulses of the challenge

Let us assume that the challenge timing resolution is typically 125 ns.

$T_{write} = 8128 * t_{ref}' + t_0$,

As the STARC and the BCM MCU are not clocked by the same oscillator, the reference periods are not the same. The STARC toggles in write mode after for T0 (maximum) or for T1 (minimum). Therefore, the time of the first challenge data is different than the other ones.

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Its length varies between the following:

- t_{max} =(8128 * t_{ref}' – T1) + t_0
- t_{min} =(8128 * t_{ref}' – T0) + t_0

In the following equations, it is assumed that the difference of the two reference periods is ε (in ppm). Thus, $t_{ref}' = t_{ref} * (1 + \varepsilon)$:

- t_{max} =(8128 * t_{ref}' – T1) + t_0 = t_0 + 64 * t_{ref} + 8128 ε t_{ref}
- t_{min} =(8128 * t_{ref}' - T0) + t_0 = t_0 - 64 * t_{ref} - 8128 ε t_{ref}

Therefore, the tolerances of the length of this first transmitted challenge pulse is about +/-(8 µs + εms).

Note that this calculation assumes that the rise time and the fall time on the K line are the same. If a capacitance was inserted on the K line, the rise edge would be controlled by the combination of the pull-up resistor and this capacitance; whereas the fall time would be very short. Therefore, the difference between the rise time and the fall time should be considered and subtracted to T_{write} so that the H field shut-down is t_0 +/- 8 µs. This calculation also assumes that the H field settling time and the H field shut-down time are the same (that means that the Q factor of the base station is the same when the antenna drivers are enabled and when they are disabled).

Thus, the crystal accuracy of the STARC and the BCM MCU must be so that the tolerances of this transmitted challenge pulse are compatible with the transponder specification. If we assume that the BSM MCU crystal is much more accurate than the STARC oscillator, ε is defined by the tolerance of the STARC oscillator. Let us consider a +/- 0.2% accurate oscillator. Then the tolerances of this transmitted challenge pulse are +/-10 µs. Such a tolerance is compatible with the specification of the PFC7936 transponder because the tolerance of the low field time is +/-24 µs.

Note that this timing is not exactly true as it does not include the time which is needed by the BCM MCU to detect the falling edge before starting the write command. This is supposed to be negligible; else it must be considered in the T_{write} timing.

Write to Read Switching

Switching from write to read is not an issue. As a matter of fact, the PFC7936 transponder starts to answer at least 1.648 ms after the challenge being fully transmitted.

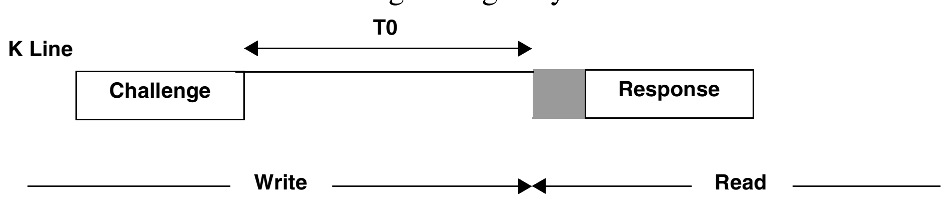

Figure 4.

After the challenge, the BCM MCU lets the K line free so that it is pulled high. After T0 or T1, the STARC toggles into read mode. The H field will not be modulated for 1.648ms –T1 = 0.656 ms. During that time, the K line level is unknown. But even if the K line was forced low by the STARC, this time is not long enough to allow the STARC to switch into write mode. Thus, after a challenge, the STARC will be in read mode when the response will be received.

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